Claims

1. A non-integer fractional divider (200) for dividing a reference clock signal 'Fvco' of period 'P' by a non-integer ratio 'K', the non-integer ratio being decomposed into an integer part 'I' and a non-integer part 'X', the non-integer fractional divider comprising:

first and second receiving means (202,203) for respectively receiving an identical plurality 'N' of clock signals 'Fvco_0 to Fvco_(N-1)', each clock signal having a period of 'P' and being equally phase shifted by a 'P/N' delay one over the other and wherein the first clock signal 'Fvco_0' being in phase with the reference clock signal;

means (201) coupled to the first and second receiving means (202,203) for selecting a first clock signal 'PHI1' from the first receiving means and a second clock signal 'PHI2' from the second receiving means;

means (205) for detecting the end of a (I-i)th period, wherein 'i' is a predetermined value;

means (204) coupled to the first and second receiving means (202,203) and to the detection means (205) for combining said first and second selected clock signals (PHI1,PHI2) to generate a clock signal 'Clock' being phase shifted by the non-integer part value 'X' of the non-integer ratio; and

means (205) coupled to the combining means (204) for dividing the shifted clock signal by the integer part 'I' of the non-integer ratio.

2. The non-integer fractional divider of claim 1 wherein the first and second receiving means respectively comprise a first multiplexer to receive the plurality 'N' of clock signals 'Fvco_0' to Fvco_(N-1)' and to output the first selected clock signal 'PHI1' in response to the selection means and a second multiplexer to receive the duplicate set 'Fvco_0 to Fvco_(N-1)' of the plurality 'N' of clock signals and to output the second selected clock signal 'PHI2' in response to the selection means.

3. The non-integer fractional divider of claim 1 wherein the selection means (201) comprises an accumulator circuit (405) to generate address selection signals (Sel1,Sel2).

4. The non-integer fractional divider of claim 1 wherein the dividing means (205) further comprising means for storing the integer value 'I' of the non-integer ratio 'K'.

5. The non-integer fractional divider of anyone of claim 1 wherein the predetermined value 'i' for detecting the end of a (I-i)th period is equal to 2.

6. The non-integer fractional divider of anyone of claim 1 wherein the selection means (201) further comprising means for storing the non-integer value 'X' of the non-integer ratio 'K'.

7. The non-integer fractional divider of anyone of claim 1 wherein the shifted clock signal 'Clock' is active during a first time period equal to the (I-2)th period and inactive during a second time period equal to $(1.5+X)$ of the (I-1)th period and active during a third time period equal to half the Ith period.

8. The non-integer fractional divider of anyone of claim 1 further comprising means (101) for dividing the reference clock signal 'Fvco' into a plurality of equally phase-shifted clock signals 'Fvco-0 to Fvco-(N-1)'.

9. The non-integer fractional divider of anyone of claim 1 wherein the combining means (204) comprises means (401,402,403,404) for detecting rising or falling edges of the selected clock signals (PHI1,PHI2).

10. A Phase Lock Loop circuit comprising the non-integer fractional divider of anyone of claim 1.

11. A method for dividing by a non-integer ratio 'K' a clock signal 'Fvco' having a period 'P', comprising the steps of:

receiving a plurality 'N' of clock signals 'Fvco_0 to Fvco_(n-1)', each clock signal having a period of 'P' and being equally phase shifted by a 'P/N' delay one over the other;

selecting a first and a second clock signals between the plurality 'N' of clock signals 'Fvco_0 to Fvco_(n-1)';

combining the first and the second selected clock signals to output a divided clock signal 'Fvco/K' such that the phase shift delay between the two selected clock signals is representative of the non-integer value of the ratio 'K'.